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Patent No. 6,934,760

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Name of Patentee: Westbrook et al.

Patent Title: METHOD AND APPARATUS FOR RESEQUENCING OF PACKETS INTO AN ORIGINAL ORDERING USING MULTIPLE RESEQUENCING COMPONENTS

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service on the date shown with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on August 30, 2005.

Kirk D. Williams, Esq. 8/30/05

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR PATENT OFFICE MISTAKE (37 C.F.R. § 1.322)

Attn: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate
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of Correction

Dear Sir:

It is requested that a Certificate of Correction be issued to correct Office mistakes found the above-identified patent. Attached hereto is a Certificate of Correction which indicates the requested correction. For your convenience, also attached are copies of selected pages (a) from the issued patent with errors highlighted, and (b) from the original application as filed February 4, 2001.

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In re US Patent No. 6,934,760

It is believed that there is no charge for this request because applicant or applicants were not responsible for such error, as will be apparent upon a comparison of the issued patent with the application as filed or amended. However, the Assistant Commissioner is hereby authorized to charge any fee that may be required to Deposit Account No. 501430.

Respectfully submitted,
The Law Office of Kirk D. Williams

Date: August 30, 2005

By _____ 8/30/05

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,934,760

DATED : Aug. 23, 2005

INVENTOR(S) : Westbrook et al.

It is certified that error(s) appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 6, line 26, replace "1115" with -- 115 --

Col. 11, line 28, replace "table 43 IA" with -- table 431 A --

Col. 15, line 19, replace "thereof" with -- thereof. --

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⇨ NONE (0)

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which communicate and coordinate actions among themselves. The reassembly components distribute information as to received packets and coordinate the sending of packets from themselves so as to produce the reassembled larger packets. In one embodiment, each of the multiple reassembly components maintains one or more data structures indicating packets stored locally and those packets stored anywhere (or elsewhere) within the multiple reassembly components. When all packets comprising a larger packet are received by one of the distributed resequencing components, the reassembly components transmit their packets typically over a common bus or link in a coordinated fashion as to produce the original larger packet.

Details of Exemplary Embodiments

FIGS. 1A–1D and their discussion herein are intended to provide a description of various exemplary embodiments and operating environments in which the invention may be practiced. FIG. 1A illustrates an embodiment including a computer system resequencing and/or reassembling packets according to the invention. FIGS. 1B–D illustrate embodiments including various packet switching systems resequencing and/or reassembling packets according to the invention.

FIG. 1A illustrates a block diagram of one embodiment of a device **100** with resequences or reassembles a received one or more streams of packets. Embodiments of device **100** include a routers, computer systems, other communications devices, etc., or components thereof. As shown, device **100** includes processor and/or control logic **102** (hereinafter "processor"), memory **101**, storage devices **104**, network interface(s) **105**, and one or more internal communications mechanisms **103** (shown as a bus for illustrative purposes). In one embodiment, processor **102** controls the operations of device **100** to resequence and/or reassemble packets according to the invention. Memory **101** is one type of computer-readable medium, and typically comprises random access memory (RAM), read only memory (ROM), integrated circuits, and/or other memory components. Memory **101** typically stores computer-executable instructions to be executed by processor **102** and/or data which is manipulated by processor **102** for implementing resequencing and/or reassembly functionality in accordance with the invention. Storage devices **104** are another type of computer-readable medium, and typically comprise disk drives, diskettes, networked services, tape drives, and other storage devices. Storage devices **104** typically store computer-executable instructions to be executed by processor **102** and/or data which is manipulated by processor **102** for implementing resequencing and/or reassembly functionality in accordance with the invention.

In one embodiment, device **100** operates as a router, bridge, switch or other communications device attached to a communications network **107**. Packets sent from source **108** over link **109** to communications network **107** are relayed over one or more links **106** to device **100**. Device **100** receives the packets, internally routes and resequences and/or reassembles the packets according to the invention. In one embodiment, device **100** consumes the resequenced and/or reassembled stream of packets. In one embodiment, device **100** sends the resequenced and/or reassembled stream of packets out one or more links **106** to destination **112**, which receives these packets from communications network **107** over link **111**.

In one embodiment, device **100** operates as a computer or communications system which receives from source **108** an out of order stream of packets and/or disassembled stream of packets. Device **100** receives the packets and resequences and/or reassembles the packets according to the invention. In one embodiment, device **100** consumes the resequenced and/or reassembled stream of packets. In one embodiment, device **100** sends the resequenced and/or reassembled stream of packets out to destination **112**.

FIGS. 1B–D illustrate the basic topology of different exemplary packet switching systems resequencing and/or reassembling packets according to the invention. FIG. 1B illustrates an exemplary packet switch **115** having multiple inputs and outputs and a single interconnection network **120**. FIG. 1C illustrates an exemplary packet switch **140** having multiple interconnection networks **141** and folded input and output interfaces **149**. FIG. 1D illustrates an exemplary folded packet switch **160** having multiple interconnection networks **161** and folded input and output interfaces **169**. Embodiments of each of these packet switches **115**, **140** and **160** resequencing and/or reassembling packets according to the invention in the manners disclosed herein along with all possible embodiments within the doctrine of equivalents. Of course, the invention is not limited to these illustrated operating environments and embodiments, and the packet switching systems may have more or less elements.

FIG. 1B illustrates an exemplary embodiment of a packet switch **1115**. Packet switch **115** comprises multiple input interfaces **117**, interconnection network **120**, and output interfaces **129**. Input interfaces **117** and output interfaces **129** are both coupled over multiple links to interconnection network **120**. Line cards **116** and **131** are coupled to input interfaces **117** and output interfaces **131**. In some embodiments including other packet switching topologies, line cards or their functionality may be included in the packet switch itself, or as part of the packet switching system.

115

In one embodiment, interconnection network **120** comprises multiple switch elements SE-1 **122**, SE-2 **125**, and SE-3 **128** that are interconnected by multiple links. Line cards **116** and **131** may connect to other systems (not shown) to provide data items (e.g., packets) to be routed by packet switch **115**. Although resequencing and reassembly of packets can be accomplished in other components in accordance with the invention, typically packets are resequenced and/or reassembled in output interfaces **129**.

FIG. 1C illustrates another exemplary operating environment and embodiment of a packet switch **140**. Packet switch **140** comprises multiple folded input and output interfaces **149** interconnected over multiple links to interconnection networks **141**, which are interconnected over multiple links returning to input and output interfaces **149**. In one embodiment, interconnection networks **141** comprise multiple switch elements SE-1 **142**, SE-2 **145**, and SE-3 **148** also interconnected by multiple links. Interfaces **149** may connect via bi-directional links to line cards **139** that connect with other systems (not shown) to provide data items (e.g., packets) to be routed by packet switch **140**. Although resequencing and reassembly of packets can be accomplished in other components in accordance with the invention, typically packets are resequenced and/or reassembled in input/output interfaces **149**.

FIG. 1D illustrates another exemplary operating environment and embodiment of a packet switch **160**. Packet switch **160** has a folded network topology. Packet switch **160** comprises multiple folded input and output interfaces **169** interconnected over multiple links to interconnection networks **161**, which are interconnected over multiple links returning to interfaces **169**. In one embodiment, intercon-

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FIG. 3 illustrates one embodiment of a mechanism for distributed resequencing and reassembly of packets in the context of a packet switching system **300**. In this exemplary embodiment, packets are distributed by a packet switch **301**, such as an eight plane packet switch, to four distributed resequencing and reassembly components **303**A–D. In one embodiment, each of two planes of the packet switch **301** are connected to one of the distributed resequencing and reassembly components **303**A–D over links **302**A–H. Distributed resequencing and reassembly components **303**A–D communicate and coordinate the resequencing and reassembly operations over ring **304**A–D. In a coordinated fashion, distributed resequencing and reassembly components **303**A–D send packets on packet merge bus **305**B–E to produce the resequenced and reassembled packets. The operation of a distributed resequencing and reassembly components **303**A–D are further described in relation to FIGS. 4A–D, 5–8.

One embodiment of distributed resequencing and reassembly component **303**B (FIG. 3) is shown in FIG. 4A. Packets are received by the packet memory manager over links **302**C–D from the packet switch **301**. An exemplary format of such packets is illustrated in FIG. 4B. A packet **430** includes a cell header **431** and cell payload **432**. The cell header has various fields, including a packet type, source, destination, fabric priority, sequence number, packet length, reserved field, and cyclic redundancy check or error-correcting code value as illustrated in table 43 IA. The packet payload **432** may contain part or all of one or two packets (e.g., a single 96 byte packet **432**A or two 48 byte packets **433**–**434**) in a payload **432**B. Of course, FIG. 4B illustrates one of numerous packet formats which may be in embodiments of the invention.

table 431A

Packet memory manager **420** maintains the packet payloads and sends the received packet headers to the packet resequencer **402** over link **419**. In addition, packet memory manager **420** receives a data structure representing a reassembled packet from packet reassembler **410** over link **418**. Packet memory manager then retrieves from memory any packet payloads stored locally corresponding to the reassembled packet. Each of the distributed resequencing and reassembly components **303**A–D places packets on the packet merge bus **305**B–**305**E to generate the reassembled packet, which is sent out packet merge bus **305**E to another component or device.

The operation of one embodiment of packet memory manager **420** is illustrated in FIG. 7. Incoming packets are received on links **302**C–D and placed in incoming packet queues **713**. Packets are then removed from incoming packet queues **713** and sent to the packet data memory controller **715**. The packet payloads are then stored in packet data memory **717**. The packet headers are simultaneously sent by packet data memory controller **715** over link **419** to packet resequencer (FIG. 4A). The operation of the other elements of packet memory manager **420** will be described hereinafter in relation to the packet merge process.

Packet resequencer **402** receives these packet headers and operates in conjunction with the packet resequencers of the other distributed resequencing and reassembly components **303**A,C–D. In one embodiment, packet resequencer **402** uses a local and a global data structures to resequence packets.

FIG. 4C illustrates one embodiment of these data structures. A local data structure **440** is used to identify packets which are received and locally stored. Local data structure **440** may take the form of a ring buffer **442** with a current position pointer **444** which is updated using the current sequence number. Ring buffer **442** could be implemented using a linked list, array, or other data structure format. Ring buffer **442** has numerous buckets **443**A–H (only eight are shown for illustration convenience) with the number of buckets typically related to the size of the out of order window. An example of an bucket entry **447** includes a packet header field **448** and payload pointer field **449**. The packet header field **448** will contain the received packet header fields, and the payload pointer points to the corresponding packet payload **449** stored in the packet memory manager **420**. Newly received packet headers are placed in local data structure **440** at a bucket position offset from the current position pointer **444** based on the sequence number of the received packet header and the sequence number corresponding to the current position pointer **444**.

A global data structure **450** is used to identify packet headers which are stored in any of the distributed resequencer and reassembly components **303**A–D (or at least the other distributed resequencer and reassembly components **303**A,C–D as the locally stored packet headers are identified in local data structure **440**). Global data structure **450** may take the form of a ring buffer **452** with a current position pointer **454** which is updated using the current sequence number. Ring buffer **452** could be implemented using a linked list, array, or other data structure format. Ring buffer **452** has numerous buckets **453**A–H (only eight are shown for illustration convenience) with the number of buckets typically related to the size of the out of order window. In one embodiment, each of the buckets **453**A–H contains a binary flag to represent whether a corresponding packet header is stored in any of the distributed resequencer and reassembly components **303**A–D (or at least the other distributed resequencer and reassembly components **303**A, C–D).

Packet resequencer **402** coordinates its activities with the packet resequencers via the communication ring **304**B, **404**, **304**C, and packet reassembler **410** communicates with the other packet reassembler over this ring **304**B, **404**, **304**C. Periodically, packet resequencer **402** sends global update information to the other packet resequencers to identify the packet headers stored locally. Referencing the local and global data structures **440**, **450** (FIGS. 4C–D) to determine what packets have been received by the distributed resequencing and reassembly components **303**A–D (FIG. 3), packet resequencer **402** can produce a stream of resequenced packet headers over link **405** to packet reassembler **410**.

One embodiment of packet resequencer **402** is further described in relation to FIG. 5. The operation of packet resequencer **402** is controlled by control logic **510** which is interconnected with other elements via communications link **511**. Embodiments of communications link **511** include most any communications mechanism, such as, but not limited to a bus, fully connected mesh, point-to-point links, etc. Control logic **510** process cell resequencing, stores and computes new resequencing state information based on information updates received from other distributed resequencer and reassembly components **303**A,C–D, and sends updates to other distributed resequencer and reassembly components **303**A,C–D.

Update messages representing the packets stored in the other distributed resequencer and reassembly components **303**A,C–D are received over ring **304**B and placed in input queue **502**, and outgoing update messages are placed in output queue **506** and sent out over link **404**. The local and global data structures **440**, **450** (FIGS. 4C–D) are updated and stored in data structure cache RAM **514**. In one

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packet descriptor to outgoing packet queues **705**. Reassembled and partially reassembled packets arrive at outgoing packet queues **705** on link **305**B. Each packet has a sequence number associated with it, and if a packet in outgoing packet queues **705** has a sequence number with a lower value, it is sent out on link **305**C before the incoming packet. Otherwise, the incoming packet is passed through.

In view of the many possible embodiments to which the principles of our invention may be applied, it will be appreciated that the embodiments and aspects thereof described herein with respect to the drawings/figures are only illustrative and should not be taken as limiting the scope of the invention. For example and as would be apparent to one skilled in the art, many of the process block operations can be re-ordered to be performed before, after, or substantially concurrent with other operations. Also, many different forms of data structures could be used in various embodiments. The invention as described herein contemplates all such embodiments as may come within the scope of the following claims and equivalents thereof

thereof.

What is claimed is:

1. A system for resequencing a stream of packets comprising:

a plurality of distributed resequencing components, each of the plurality of distributed resequencing components including one or more data structures for maintaining an indication of packets of the stream of packets that are stored in other distributed resequencing components of the plurality of distributed resequencing components;

a communications mechanism coupled to the plurality of distributed resequencing components to allow communication among the plurality of distributed resequencing components; and

one or more packet merging mechanisms coupled to the plurality of distributed resequencing components to receive packets of the stream of packets to produce a resequenced stream of the stream of packets.

2. The system of claim **1**, further comprising a distributor for distributing the stream of packets to the plurality of distributed resequencing components.

3. The system of claim **2**, wherein the distributor includes a plurality of paths through a packet switching system.

4. The system of claim **3**, wherein at least two of the plurality of path are on different planes of the packet switching system.

5. The system of claim **1**, wherein the communications mechanism includes a communication ring or bus.

6. The system of claim **1**, wherein the one or more packet merging mechanisms includes a packet merge bus.

7. A packet switching system including the system of claim **1**.

8. A router including the system of claim **1**.

9. A system for resequencing a stream of packets comprising:

a plurality of means for resequencing the stream of packets, each of the plurality of means for resequencing the stream of packets including a data structure means for indicating which packets of the stream of packets are located in other of the plurality of means for resequencing the stream of packets;

a communications means coupled to the plurality of means for resequencing the stream of packets; and

a merging means for receiving packets from the plurality of means for resequencing the stream of packets and for producing a resequenced stream of the stream of packets.

10. The system of claim **9**, further comprising a packet switching means, connected to the plurality of means for resequencing the stream of packets, for distributing packets of the stream of packets to the plurality of means for resequencing the stream of packets.

11. The system of claim **9**, wherein each of the means for resequencing the stream of packets includes a local data structure means for maintaining an indication of the packets stored locally within a particular means for resequencing the stream of packets.

12. A method for resequencing a stream of ordered packets performed by a particular component of a plurality of components, the method comprising:

receiving at least one packet of the stream of ordered packets;

receiving an indication of a set of packets received in at least one other component of the plurality of components;

maintaining one or more data structures of the set of packets received in at least one other component of the plurality of components and the received at least one packet of the stream of ordered packets;

maintaining a current position indication; and

sending a particular packet out as part of the resequenced stream based on a value of the current position indication.

13. The method of claim **12**, further comprising updating the current position indication based on the sending of the particular packet.

14. The method of claim **12**, further comprising updating the current position indication based on the received indication of the set of packets contained in the at least one other component of the plurality of components.

15. The method of claim **12**, wherein the sending of the particular packet includes coordinating the timing for sending of the particular packet with at least another component of the plurality of components.

16. The method of claim **12**, wherein the indication of the set of packets contained in the at least one other component of the plurality of components is received over a communications ring or bus.

17. The method of claim **12**, further comprising sending an update indication identifying the sent particular packet to one or more of the other components of the plurality of components.

18. The method of claim **17**, wherein the update indication includes a sequence identifier of the sent particular packet.

19. The method of claim **12**, wherein each of the packets of the stream of ordered packets is identified with a sequence identifier.

20. The method of claim **19**, wherein the sequence identifier is a sequence number or a timestamp value.

21. The method of claim **12**, further comprising storing the received at least one packet on a storage device or in a memory; and retrieving the received at least one packet from the storage device or the memory.

22. A packet switching system performing the method of claim **12**.

23. A router performing the method of claim **12**.

24. A computer system performing the method of claim **12**.

* * * * *

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From Patent Application Filed Feb. 4, 2001

packets according to the invention in the manners disclosed herein along with all possible embodiments within the doctrine of equivalents. Of course, the invention is not limited to these illustrated operating environments and embodiments, and the packet switching systems may have more or less elements.

FIG. 1B illustrates an exemplary embodiment of a packet switch 115. Packet switch 115 comprises multiple input interfaces 117, interconnection network 120, and output interfaces 129. Input interfaces 117 and output interfaces 129 are both coupled over multiple links to interconnection network 120. Line cards 116 and 131 are coupled to input interfaces 117 and output interfaces 131. In some embodiments including other packet switching topologies, line cards or their functionality may be included in the packet switch itself, or as part of the packet switching system.

In one embodiment, interconnection network 120 comprises multiple switch elements SE-1 122, SE-2 125, and SE-3 128 that are interconnected by multiple links. Line cards 116 and 131 may connect to other systems (not shown) to provide data items (e.g., packets) to be routed by packet switch 115. Although resequencing and reassembly of packets can be accomplished in other components in accordance with the invention, typically packets are resequenced and/or reassembled in output interfaces 129.

FIG. 1C illustrates another exemplary operating environment and embodiment of a packet switch 140. Packet switch 140 comprises multiple folded input and output interfaces 149 interconnected over multiple links to interconnection networks 141, which are interconnected over multiple links returning to input and output interfaces 149. In one embodiment, interconnection networks 141 comprise multiple switch elements SE-1 142, SE-2 145, and SE-3 148 also interconnected by multiple links. Interfaces 149 may connect via bi-directional links to line cards 139 that connect with other systems (not shown) to provide data items (e.g., packets) to be routed by packet switch 140. Although resequencing and reassembly of packets can be accomplished in other components in accordance with the invention, typically packets are resequenced and/or reassembled in input/output interfaces 149.

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to one of the distributed resequencing and reassembly components 303A-D over links 302A-H. Distributed resequencing and reassembly components 303A-D communicate and coordinate the resequencing and reassembly operations over ring 304A-D. In a coordinated fashion, distributed resequencing and reassembly components 303A-D send packets on packet merge bus 305B-E to produce the resequenced and reassembled packets. The operation of a distributed resequencing and reassembly components 303A-D are further described in relation to FIGs. 4A-D, 5-8.

One embodiment of distributed resequencing and reassembly component 303B (FIG. 3) is shown in FIG. 4A. Packets are received by the packet memory manager over links 302C-D from the packet switch 301. An exemplary format of such packets is illustrated in FIG. 4B. A packet 430 includes a cell header 431 and cell payload 432. The cell header has various fields, including a packet type, source, destination, fabric priority, sequence number, packet length, reserved field, and cyclic redundancy check or error-correcting code value as illustrated in table 431A. The packet payload 432 may contain part or all of one or two packets (e.g., a single 96 byte packet 432A or two 48 byte packets 433-434) in a payload 432B. Of course, FIG. 4B illustrates one of numerous packet formats which may be in embodiments of the invention.

Packet memory manager 420 maintains the packet payloads and sends the received packet headers to the packet resequencer 402 over link 419. In addition, packet memory manager 420 receives a data structure representing a reassembled packet from packet reassembler 410 over link 418. Packet memory manager then retrieves from memory any packet payloads stored locally corresponding to the reassembled packet. Each of the distributed resequencing and reassembly components 303A-D places packets on the packet merge bus 305B-305E to generate the reassembled packet, which is sent out packet merge bus 305E to another component or device.

The operation of one embodiment of packet memory manager 420 is illustrated in FIG. 7. Incoming packets are received on links 302C-D and placed in incoming packet queues 713. Packets are then removed from incoming packet queues 713 and sent to the

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With regards to FIG. 7, packets arrive on links 302 C-D and are temporarily stored in incoming packet queues 713. Packets are forwarded from incoming packet queues 713 to packet data memory controller 715. Packet data memory controller 715 allocates memory for the packet, stores the packet in packet data memory 717, and forwards the packet header which contains a pointer to the packet to resequencing engine 402 (FIG. 5) over link 419.

When packets are de-queued, a stream of packet descriptors arrive at packet merge queue 701 over link 418. Packet merge queue 701 forwards the packet pointers to packet data memory controller 715 which reads the packet out of packet data memory 717 and forwards it to the outgoing packet queues 705. Packet merge queue 701 also forwards the packet descriptor to outgoing packet queues 705. Reassembled and partially reassembled packets arrive at outgoing packet queues 705 on link 305B. Each packet has a sequence number associated with it, and if a packet in outgoing packet queues 705 has a sequence number with a lower value, it is sent out on link 305C before the incoming packet. Otherwise, the incoming packet is passed through.

In view of the many possible embodiments to which the principles of our invention may be applied, it will be appreciated that the embodiments and aspects thereof described herein with respect to the drawings/figures are only illustrative and should not be taken as limiting the scope of the invention. For example and as would be apparent to one skilled in the art, many of the process block operations can be re-ordered to be performed before, after, or substantially concurrent with other operations. Also, many different forms of data structures could be used in various embodiments. The invention as described herein contemplates all such embodiments as may come within the scope of the following claims and equivalents thereof.

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